Fig. 7(a)

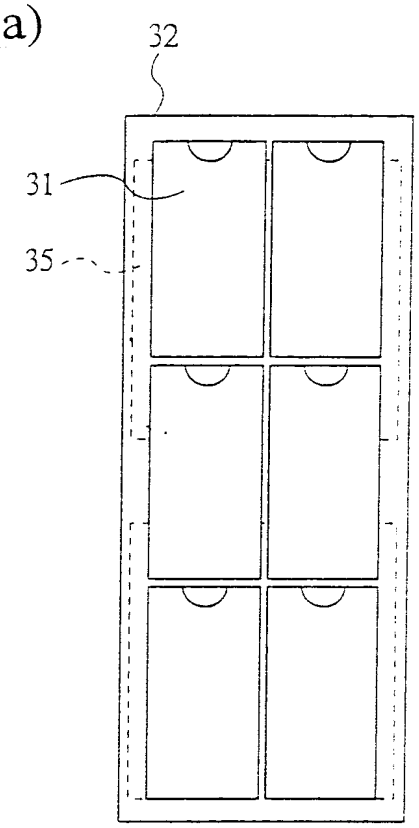

Fig. 7(b)

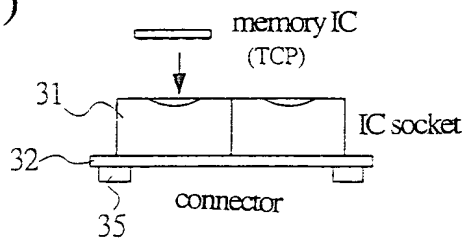

Fig. 14

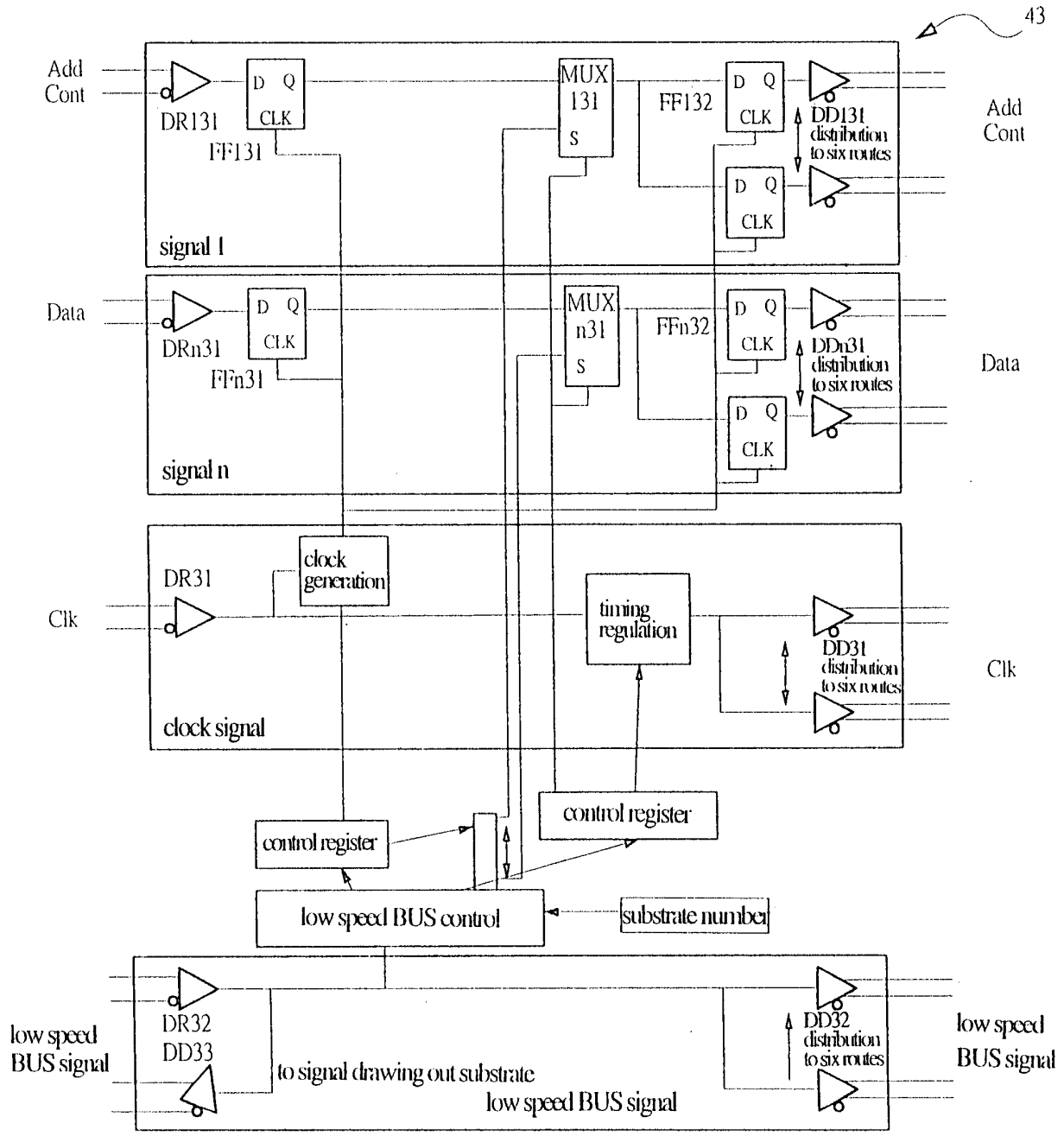
43
Add Cont
DR131
D Q
CLK
FF131
MUX 131
S
FF132
DD131 distribution to six routes
signal 1
Data
DRn31
FFn31
MUX n31
FFn32
DDn31 distribution to six routes
signal n
DR31
clock generation
Clk
timing regulation
DD31 distribution to six routes
clock signal
control register
low speed BUS control
substrate number
low speed BUS signal
DR32
DD33
to signal drawing out substrate
low speed BUS signal
DD32 distribution to six routes

Fig. 15

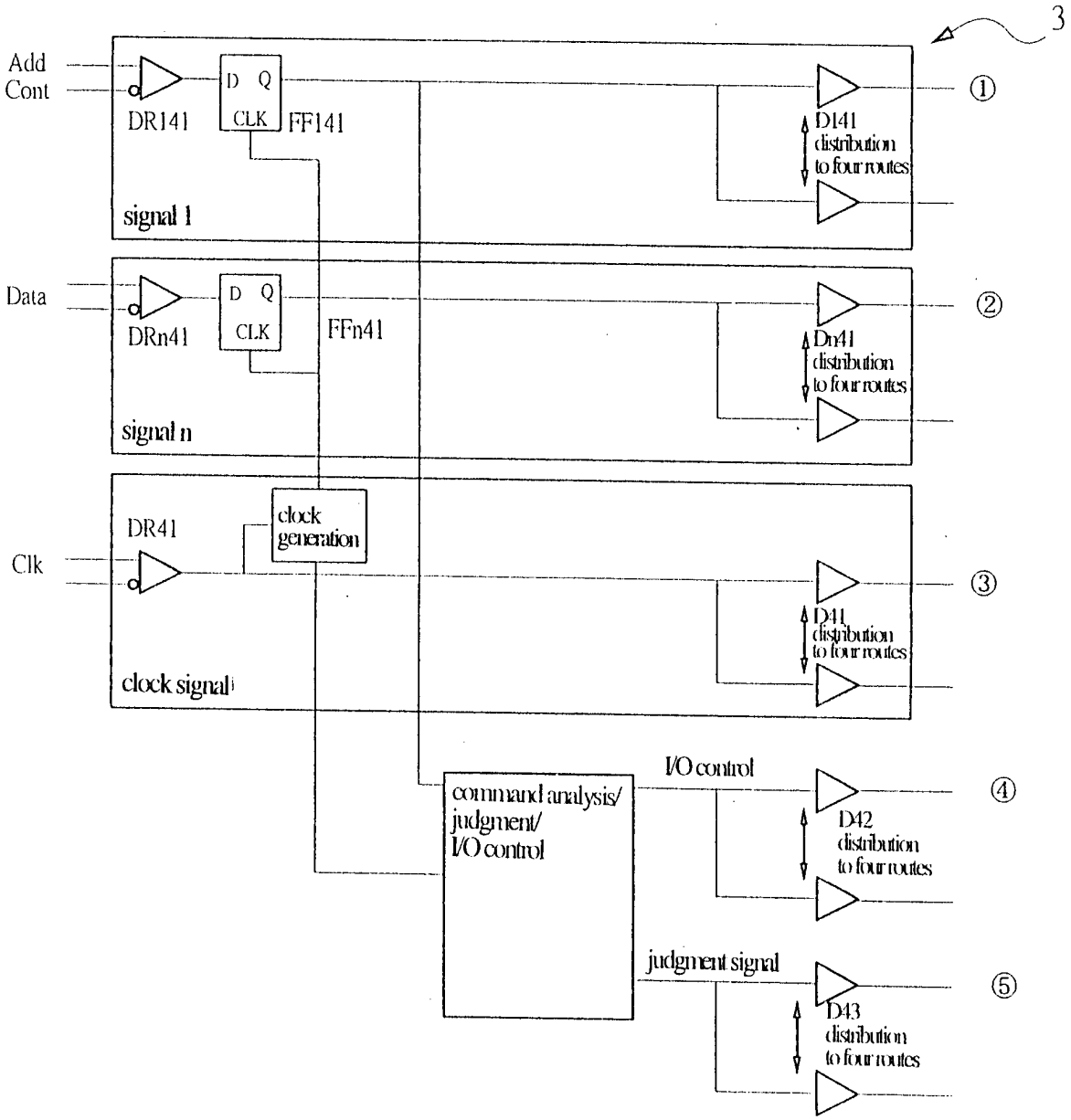
3
Add
Cont
DR141
D Q
CLK
FF141
signal 1
D141
distribution
to four routes
①
Data
DRn41
D Q
CLK
FFn41
signal n
Dn41
distribution
to four routes
②
DR41
clock
generation
Clk
clock signal
D41
distribution
to four routes
③
I/O control
command analysis/
judgment/
I/O control
D42
distribution
to four routes
④
judgment signal
D43
distribution
to four routes
⑤

Fig. 16

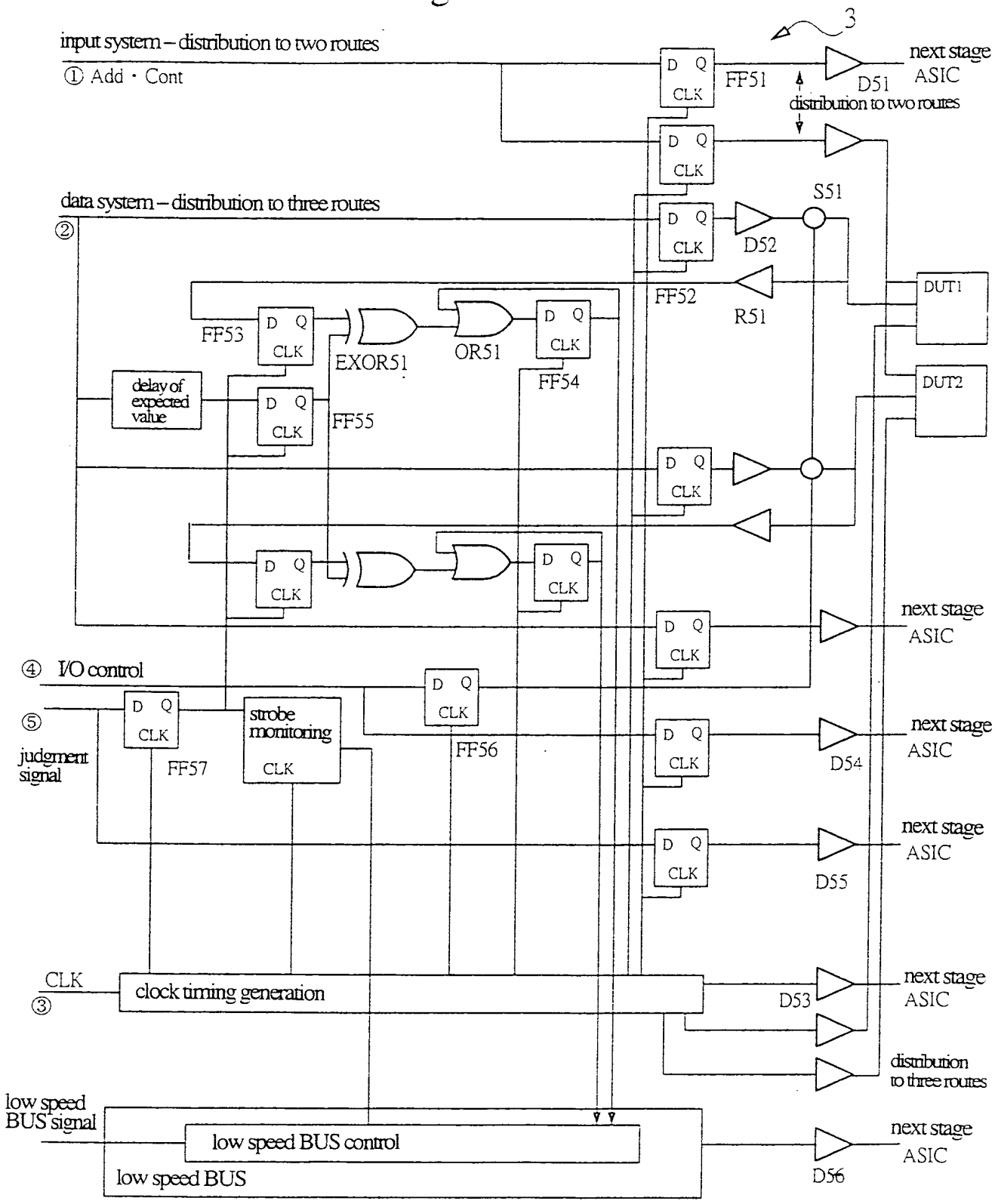
3
input system – distribution to two routes
① Add · Cont
D Q
CLK
FF51
D51
next stage
ASIC
distribution to two routes
data system – distribution to three routes
②
S51
D52
FF52
R51
DUT1
DUT2
FF53
EXOR51
OR51
FF54
delay of expected value
FF55
next stage
ASIC
④ I/O control
⑤
judgment signal
FF57
strobe monitoring
FF56
D54
D55
CLK
③
clock timing generation
D53
distribution to three routes
low speed BUS signal
low speed BUS control
low speed BUS
D56

Fig. 12